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13. ABSTRACT *(Maximum 200 words)*

This research was directed towards realization of Si monolithic microwave communication transceivers. New theoretical methods were developed for the analysis of noise and distortion phenomena in nonlinear communication circuits such as low-noise amplifiers (LNAs) in the over-driven condition, mixers, oscillators and detectors. Using these techniques new circuit topologies were synthesized for the realization of various essential transceiver functions, and prototype circuits were built in state-of-the-art Si monolithic processes and experimentally evaluated. New CAD approaches to the problem of mixer noise analysis were created which allow combination of large-signal time-varying circuit elements plus time-varying noise sources to be analyzed. Using this tool a new mixer topology in Si BiCMOS technology was synthesized with extremely wide dynamic range. The use of on-chip monolithic inductors allowed incorporation of a new tuned local-oscillator (LO) buffer circuit which added important degrees of freedom to the mixer realization.

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High-Frequency Integrated Circuits for Communication Systems

Final Progress Report

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October 16, 1997

U.S. Army Research Office

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Abstract

This research was directed towards realization of Si monolithic microwave communication transceivers. New theoretical methods were developed for the analysis of noise and distortion phenomena in nonlinear communication circuits such as low-noise amplifiers (LNAs) in the over-driven condition, mixers, oscillators and detectors. Using these techniques new circuit topologies were synthesized for the realization of various essential transceiver functions, and prototype circuits were built in state-of-the-art Si monolithic processes and experimentally evaluated. New CAD approaches to the problem of mixer noise analysis were created which allow combination of large-signal time-varying circuit elements plus time-varying noise sources to be analyzed. Using this tool a new mixer topology in Si BiCMOS technology was synthesized with extremely wide dynamic range. The use of on-chip monolithic inductors allowed incorporation of a new tuned local-oscillator (LO) buffer circuit which added important degrees of freedom to the mixer realization.

The focus of this research was on the realization of Si monolithic microwave communication transceivers. Our approach was multi-faceted. We developed new theoretical methods for the analysis of noise and distortion phenomena in nonlinear communication circuits such as low-noise amplifiers (LNAs) in the overdriven condition, mixers, oscillators and detectors. Using these techniques we synthesized and developed new circuit topologies for the realization of various essential transceiver functions, and then built and tested prototype circuits in state-of-the-art Si monolithic processes.

Mixers are important elements in communication transceivers. They perform the crucial function of frequency translation and are often the limiting element in setting both the noise figure and large-signal behavior (intermodulation and gain compression point) of the radio frequency (RF) front end. Noise analysis in mixers is complicated by the fact that the mixing process inherently requires large-signal operation of the active devices and this precludes the usual linearized approach to noise analysis. In addition, mixers based on the Gilbert Quad approach (whether using FET or bipolar active devices) contain time-varying noise sources connected across time-varying nonlinear impedances. These factors create significant complexity in the noise analysis.

Our research on monolithic mixers resulted in the development [9] of new CAD approaches to the problem of mixer noise analysis. Any combination of large-signal time-varying circuit elements plus time-varying noise sources can be analyzed. Using this tool we developed design approaches to achieve optimum performance in Gilbert-cell-based HF switching mixers. We have synthesized a new mixer topology in Si BiCMOS technology with extremely wide dynamic range. The use of on-chip monolithic inductors has allowed incorporation of a new tuned local-oscillator (LO) buffer circuit which adds important degrees of freedom to the mixer realization. Test circuits were layed out in an advanced BiCMOS technology and experimental evaluation of the test chips verified our theoretical results.

A primary goal of our research program was to find optimum paths to the realization of RF transceivers with extremely high levels of integration. We made major advances in this direction with the synthesis and fabrication [10] of a unique monolithic integrated circuit (IC) incorporating a substantial portion of the high-frequency function of a personal communication receiver. Many new concepts for RF circuits which have since become widely accepted were introduced, such as battery power-saving techniques and on-chip compensation against environmental effects such as ambient temperature and battery voltage fluctuation. The critical issues of interaction between the electronic circuit and its environment when using low-cost packaging techniques were addressed. A number of new strategies with wide application were devised for incorporating the package environment into the chip design. The influence of package-related inductive and capacitative coupling on overall circuit performance was investigated and characterized. Methods of minimizing the deleterious effects of the package were devised and circumstances were the package itself has a beneficial effect were identified and quantified. In particular, the influence of package-related supply-line inductance was characterized and various methods of on-chip supply-line bypassing were devised and implemented.

Our research on the realization of circuits with higher levels of RF integration showed that the integrated-circuit substrate can have an influence on circuit performance comparable to, or even greater than, the packaging issues described above. We found numerous instances where both theory and experiment indicated extensive circuit interaction via substrate coupling. The need to characterize and quantify these effects led us to develop new, highly-efficient algorithms for the simulation of these effects in practical RF integrated circuits [14]. The CAD program we developed takes as its input the surface layout dimensions and locations of the IC components together with substrate and device doping data. Coupling down to the substrate from arbitrary numbers of micron-sized regions is readily handled, as is the computation of pickup in adjacent

and remote regions of the chip. A lumped network representing substrate coupling is produced and layed under the electrical schematic of the circuit itself with appropriate connections between the two. The package model is then added to surround the circuit and substrate. Use of this tool has enabled us to obtain very close agreement between simulation and measured circuit performance in the presence of substrate effects. Substrate coupling in different types of substrates was analyzed and the utility of substrate guard rings was explored and defined. These results were verified by measurements on a comprehensive test chip containing many different elements with a wide range of spatial orientation. An interesting finding ws that the current widespread practice of including substrate taps more or less at random on a chip in an attempt to minimize coupling usually results in an *increase* in the problem rather than improved performance. The efficiency of these algorithms is such (orders of magnitude faster than simple schemes) that computer optimization of layouts for coupling minimization is a practical goal.

Our research in the area of low-noise high-frequency monolithic amplifiers (LNAs) led to the identification of new mechanisms limiting the large-signal performance of such circuits [13]. We showed theoretically and verified experimentally that the blocking performance of RF LNAs is directly related to the second-order intercept performance as well as the third-order intercept. Blocking performance is an important system parameter which specifies the ability of an amplifier to remain functional in the presence of large, unwanted, interfering signals. Because of the pressure to allow the maximum number of users in wireless communication systems, the problem of accidental interference from adjacent channels is a constant and growing issue. In military communication systems the interferer may be deliberately generated. The effect of third-order intermodulation products in reducing system sensitivity has long been realized, but second-order intermodulation performance is rarely specified. We showed that low-frequency noise mixed via second-order mechanisms against a single close-in interferer can have major impact on system sensitivity. Amplifier design techniques to minimize these effects were devised and quantified.

Accurate detection of on-chip signal amplitude levels is an important tool in the design of precision RF monolithic systems. This signal-level information is used to active automatic-gain-control (agc) loops, received-signal-strength indicators (RSSI) and potentially may be used to adaptively adjust on-chip circuit parameters to optimize noise and overload behavior in real time. Our research in this area led to the development and characterization of a new low-power temperature-compensated precision on-chip amplitude detector [11]. Theoretical calculations produced closed-form expressions for the detected output signal as a function of RF input and circuit parameters. Computer simulation and high-frequency measurements verified these results.

A major research topic in this program has been the realization and exploitation of on-chip inductive elements in standard silicon technologies. The successful incorporation of on-chip inductors into Si ICs in the gigahertz frequency range has resulted in major improvements in RF performance and major reductions in power dissipation. Since we introduced this concept under ARO sponsorship in 1990 many groups around the world in industry and academia have recognized its potential and incorporated on-chip inductors in a variety of Si-based applications. As part of this research project we developed CAD tools for on-chip inductor design which have generated great interest in the RF circuit-design community.

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